

Title of Paper

Next Generation Test Engine Environment for Aircraft Cabin Systems Testing

Presenter

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Session Format

Workshop Tutorial Industrial project papers Academic presentations

Possible Presentation Languages

English German

Instructional Skill Level

Introductory Intermediate Advanced

Target Group

Test practitioners and engineers, test bench designers, software and test managers, QA managers and development managers as well as other professionals interested in building and delivering complex system test environments.

Keywords

- Software Quality Management Software Testing
- Modular Test Bench Design
- Hard Real-Time Testing of Embedded Systems
- Test Administration and Management
- Automated Test Setup
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Abstract

Targeted for its first application in the cabin controller development process of the next Aircraft generation, a general purpose test environment has been developed by Airbus which provides means for single cabin system tests as well as for tests involving all cabin systems. This environment called "Testing Factory" is based on a workflow definition and the tool- and infrastructure definitions supporting this process. This abstract deals with the test engine environment as one part of the Testing Factory. It is based on small, reusable and highly configurable basic test and simulation modules, which can easily be set up and combined due to common interfaces to fit any future test bench

needs. The configuration management and control of all these simulation modules is performed via a generic configuration tool that relies on one central database. The first implementation of this test engine environment concept has been finished in cooperation of Airbus, esd electronic system design GmbH and Verified Systems International GmbH.

One major aspect of the testing engine environment concept is the idea of setting up test benches for specific systems under test (SUTs) from small building blocks, the so-called SOE modules (hardware modules, hosting simulations and test procedures and interfacing original equipment, "Simulated Original Equipment"). By using a self-sustaining SOE hardware architecture that is optimised for the application area (using COTS hardware whenever applicable) and providing a common interface for configuration and interconnection of several SOEs, they provide a high flexibility (the test engine environment can easily be adapted to a change of the test approach) combined with a low total cost of ownership. A single SOE module is designed for performing hard real-time hardware-in-the-loop black box testing and/or simulation of reactive systems. The SOE is based on COTS hardware components and several customised I/O boards have been developed, which provide all specific functions necessary for the cabin controller tests. The available hardware I/Os of an SOE are easily changeable by insertion of different I/O boards; a plug and play mechanism for the detection of available I/Os and their characteristics eases the test bench adaptation in case of additional I/O requirements of the SUT. In case of defective hardware this feature minimises the downtime of test benches. The SOEs and its hardware are highly configurable, for example with respect to I/O characteristics and signal conditioning, thus allowing for an adaptation to very different SUT needs.

With regard to the configuration of SOE modules and the communication of test data between SOE modules building a current test bench setup, a public interface description was defined by Airbus, esd and Verified Systems. This comprises definitions for

- SOE configuration setups and configuration reporting. Such information is exchanged between the SOE and the generic configuration tool when setting up a test by using so-called Inventory Reports which are XML documents.
- Signal data communication. This makes it possible to set up heterogeneous networks of different modules (e.g. modules from different providers, panel systems, data logger etc.)
- Log message interfaces, including health monitoring and status information for SOE control during a test execution.

Legacy test benches can be integrated into the test engine environment by using the corresponding integration layers since it is also possible to integrate components that only provide a subset of the described SOE features.

Another main feature of the test engine environment is the possibility to interconnect SOEs among each other and to other components via the signal data interface. Each Signal data transferred within or between SOEs is transferred via so-called Process Variables (PVs) between a PV producer and consumer. This signal abstraction does not distinguish between simulation and hardware signals or between signals that are communicated within or between SOEs. Therefore, the access to (hardware) I/Os from simulations or test procedures is independent of the actual I/O type.

The PV based routing and signal assignment is part of the SOE XML configuration. Therefore, simulations and test procedures may be defined independently from hardware characteristics. The concrete signal routing within a test session is set up automatically during test start-up by using a publisher/subscriber protocol in order to reduce the load of the PV data exchange networks to the necessary minimum.

The test engine environment is designed to be scalable to all levels – from single system tests (controllers of one A/C system), multi system tests, to complete aircraft cabin tests. In order to handle and maintain the configurations of all test engines and to be able to change the test engine configurations quickly from system tests to multi system tests, a Generic Test Session Configuration Tool (GSECT) has been developed for the Test Engine environment. It offers complete control over the aspects of preparation, setup and execution of a test configuration. For this purpose the central

GSECT database contains:

- All relevant signal interface descriptions, which are mainly derived from dedicated design documents.
- A representation of all physical components of the test engine environment including all parameters necessary for the identification and configuration of the component (Systems under Test (SUT), SOE module H/W configuration etc.)
- A representation of all logical components with all parameters necessary for the identification and configuration of the component (Simulation, Test Procedures, Panels etc.)
- All test configurations (test sessions) that are concatenations of logical and physical components with a specific configuration of the components parameters and a connection definition of the respective signal interfaces.

All components of the GSECT database can either be imported from XML- or Airbus design documents and/or created and modified directly in the GSECT tool.

A single graphical user interface enabling users to select and manage all GSECT components that are visualised in the form of a hierarchical view, broken down into subcomponents like SUT connectors and pins, I/O boards, simulation with layers to structure the PVs (of the simulation interface). On each level all properties of a component can be observed and modified. Furthermore, a common interface for the design and visualisation of the physical wiring and the definition of the signal data communication is available.

Applying configuration management means on all components administered within GSECT ensures the traceability of all test executions. Since the steps of preparation, setup and execution of a test configuration are performed by users with different responsibilities, a user rights management is employed defining roles with allowed operations on specific components.

Since the creation of complex test configurations is very time consuming, several functions are provided by GSECT to ease the test configuration procedure by automatisms. E.g. GSECT automatically derives the signal configuration from controller design documents and creates SOE module I/O configurations with respect to the attached physical components according to the wiring definition. Another feature is a mechanism to generate connection definitions for PVs of a test configuration based on the equivalence of signal parameters (signal name, data type etc.) of the respective output and input PVs.

Currently, the first SOE modules and the GSECT software environment have been delivered and are being evaluated and integrated at the Airbus site in Hamburg. In 2008, this test engine environment will be extended and integrated to the overall Testing Factory environment.

Biography

Malte Schwarze has studied electrical engineering at the Technical University of Hamburg-Harburg and received his diploma about the design and development of an automotive radar network to detect objects all around a car in 2005. Since 2005, he worked in the core design team developing the next generation test engine environment for the Testing Factory and took over the project lead for the GSECT tool at Airbus in 2007.

Dr. Oliver Meyer has studied computer science at the University of Bremen and received his diploma about the design, risk analysis and formal verification of safe autonomous systems in 1997. Afterwards, he worked for four years at the University of Bremen as a Research Assistant in the area of formal language based real-time testing approaches. As a member of the Bremen Institute of Safe Systems, Oliver Meyer participated in a number of real-time testing and simulation projects for avion-

ics and space controllers. He received his Ph.D. in 2001 with his work about temporal aspects of formal specification based real-time testing and their practical implications. Since 2001 he is project manager at Verified Systems International GmbH, mainly working in test projects of embedded controllers in the avionics domain. Currently, he is managing a project about the development of modular real-time test benches for safety critical systems.

Raymond Scholz has studied computer science at the University of Bremen focused on safe systems and formal verification and received his diploma about the formal specification of an aircraft cabin communication system in 2001. Afterwards, he worked as a test and verification engineer for automated hardware-in-the-loop systems at DaimlerChrysler AG. Since 2003 he is working at Verified Systems International GmbH in test projects of embedded controllers in railway systems and the avionics domain. Since 2005 he is project manager of the design and development of a generic configuration tool for real-time test benches.

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